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EXAMINER
LE, THONG QUOC

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,104	TAKAYANAGI, TOSHINARI	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,13-15,24-27,34-36,38-40 and 45-58* is/are rejected.

7)☒ Claim(s) *2-4,-12,16-23,28-33,37,41-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/04/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on August 30, 1999 has been entered.

2. Claims 1-58 are presented for examination.

Information Disclosure Statement

3. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 04/04/2006.

4. Information disclosed and list on PTO 1449 was considered.

Response to Arguments

5. Applicant's arguments with respect to claims 1-58 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1,5,13-15,24-27,34-36,38-40,45-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Eleyan et al. (Pub. U.S. Patent No. 2003/0198112).

Regarding claim 1, Eleyan et al. disclose a method of compensating for accumulated data-dependent post- manufacture shift in a characteristic of one or more of a pair of matched devices within an integrated circuit, said shift giving rise to a mismatch in the characteristic between the pair of matched devices ([0012]), the method comprising:

preconditioning the matched devices ([0005-0007], Figure 3, 300) to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift ([006-007], "right time")in the characteristic of either matched device ([0038], Claim 10).

Regarding claim 5, Eleyan et al. disclose wherein the preconditioning step is carried out at an elevated temperature to promote the shift in characteristic (ABSTRACT, [0009], [0024]).

Regarding claim 13, Eleyan et al. disclose the matched devices (Figure 2, 221,222) form a portion of a sensing circuit of a semiconductor memory (Figure 2); and the at least one characteristic susceptible to an accumulated data-dependent mismatch result, at least in part from an effect that disparately affects one of the pair of match devices as compared with the other, the disparate effect base based on a skew in a

history of values read out from associated memory elements (ABSTRACT, [0012],[0028]).

Regarding claim 14, Eleyan et al. disclose wherein the disparate effect is associated with negative bias temperature instability ([0024]).

Regarding claim 15, Eleyan et al. disclose wherein the disparate effect involves a monotonic change in the characteristic based on disparate voltage bias histories of the matched devices (Column 5, claim 4).

Regarding claim 17, Eleyan et al. disclose wherein the characteristic is threshold voltage (Vt) (Column 5, claim 4).

Regarding claims 18-19, Elayen et al. disclose wherein the pair of matched devices comprises PMOS transistors (Figure 2, 221,222) ; the characteristic is threshold voltage (Vt) (Column 5, claim 4) ; and the disparate effect is associated with negative bias temperature instability and results in a monotonic increase in Vt based on disparate voltage bias histories of the PMOS transistor devices (Column 5, claim 3).

Regarding claim 24, Eleyan et al. disclose a circuit (Figure 2) comprising:

first and second matched devices (Figure 2, 221, 222) which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices said shift giving rise to a mismatch in the characteristic between the matched devices (ABSTRACT, [0011-0012], ; and

a preconditioning circuit (Figure 3, 300) , for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected

magnitude of any further lifetime shift in the characteristic of either matched device ([0030-0031]).

Regarding claims 25-27, Elayen et al. disclose wherein the first and second matched devices together comprise a cross-coupled pair of transistors within a sensing circuit of a semiconductor memory (Figure 2), and the cross-coupled pair of transistor comprises PMOS transistors (Figure 2, 221, 222), and wherein the preconditioning circuit comprises means for applying a substantially uniform bias history across both first and second matched devices (ABSTRACT)

Regarding claims 34-36, 38, Elayen et al. disclose wherein the at least one characteristic susceptible to an accumulated data-dependent mismatch results, at least in part, from an effect that disparately affects one of the pair of matched devices as compared with the other, the disparate effect based on a skew in a history of values read out from associated memory elements (Column 5, claim 4), and wherein the disparate effect is associated with negative bias temperature instability (Column 5, claim 3), and wherein the disparate effect involves a monotonic change in the characteristic based on disparate voltage bias histories of the matched devices (Column 5, claim 4), and wherein the characteristic is threshold voltage (Vt) (Column 5, claim 4)

Regarding claims 39-40, Elayen et al. disclose wherein the pair of matched devices comprises PMOS transistors (Figure 2, 221,222) ; the characteristic is threshold voltage (Vt) (Column 5, claim 4) ; and the disparate effect is associated with negative bias temperature instability and results in a monotonic increase in Vt based on disparate voltage bias histories of the PMOS transistor devices (Column 5, claim 3).

Regarding claim 45, Elayen et al. disclose a sensing circuit of a memory integrated circuit (ABSTRACT, Figure 2).

Regarding claim 46, Elayen et al. disclose embodied within a sensing of a processor integrated circuit including memory or cache ([0004], Column 6, claim 37).

Regarding claim 47, Elayen et al. disclose embodied as a sensing circuit in computer readable descriptive form suitable for use in design, test, or fabrication of an integrated circuit ([0013], [0015], Column 6, claim 32).

Regarding claim 48, Aleyan et al. disclose an integrated circuit (Figure 2) comprising:

memory elements (ABSTRACT);

a sense amplifier circuit (Figure 2) for sensing data stored in associated memory elements, said sense amplifier including first and second matched devices which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices ([0016-0017]); and

a preconditioning circuit (Figure 3) for subjecting the matched devices to a particular condition for a length of time sufficient ([0006-0007], right time) to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device ([0006]).

Regarding claims 49-51, Aleyan et al. disclose wherein the first and second matched devices together comprise a cross-coupled pair of transistors within a sensing

circuit of a semiconductor memory (Figure 2), and wherein: the cross-coupled pair of transistors comprise PMOS transistors (Figure 2, 221,222), and wherein the at least one characteristic susceptible to an accumulated data-dependent mismatch results, at least in part, from an effect that disparately affects one of the first load devices as compared with the other, the disparate effect based on skew in a history of values read out from associated memory element ([0012]).

Regarding claim 46, Elayen et al. disclose wherein the disparate effect is associated with negative bias temperature instability (Column 5, claim 4).

Regarding claims 53, Elayen et al. disclose wherein the pair of matched devices comprises PMOS transistors (Figure 2, 221,222) ; the characteristic is threshold voltage (Vt) (Column 5, claim 4) ; and the disparate effect is associated with negative bias temperature instability and results in a monotonic increase in Vt based on disparate voltage bias histories of the PMOS transistor devices (Column 5, claim 3).

Regarding claim 54, Elayen et al. disclose embodied within a sensing of a processor integrated circuit including memory or cache ([0004], Column 6, claim 37).

Regarding claim 55, Elayen et al. disclose embodied as a sensing circuit in computer readable descriptive form suitable for use in design, test, or fabrication of an integrated circuit ([0013], [0015], Column 6, claim 32).

Regarding claim 56, Aleyan et al. disclose a computer readable encoding of a semiconductor integrated circuit design, the computer readable encoding (Columns 6-7, claim 40), comprising:

one or more media encoding a representation of a memory circuit that includes plural pairs of bit lines, memory cells coupled to respective ones of the bit line pairs; the one or more media further encoding a representation of a sense amplifier circuit coupled to one or more respective ones of the bit line pairs for sensing data stored in associated memory elements, said sense amplifier circuit including first and second matched devices which are susceptible to an accumulate data-depend post manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices; and

the one or more media further encoding a representation of a preconditioning circuit (Figure 3) for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device (Column 7, claim 40, preconditioning circuit is Figure 3, and length of time is right time).

Regarding claim 57, Aleyan et al. disclose wherein each of the one or more media are selected from the set of a disk, tape or other magnetic, optical semiconductor or electronic storage medium and a network, wireline, wireless or other communications medium (Column 7, claim 41).

Regarding claim 58, Aleyan et al. disclose in combination with one or more respective media readers therefor, wherein the one or more media and respective media readers, when combined, are exercisable to supply an information steam suitable

to at least partially define one or more process steps for fabrication of semiconductor integrated circuits in accordance with the encoded design (Column 7, claim 42).

Allowable Subject Matter

8. Claims 2-4,6-12,16,20-23, 28-33, 37, 41-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-4,6-13,16,20-23, 28-33,41-44 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Eleyan et al. (Pub. U.S. Patent No. 2003/0198112), and others, does not teach the claimed invention having wherein the respective initial shift in each of the matched devices is substantially equal as claims 2 disclosed, and wherein the respective initial shift in the characteristic in each of the matched devices is greater than the an expected magnitude of any remaining lifetime shift in the characteristic of either matched devices as claims 3-4,6-8, 10-12, and wherein the preconditioning step is performed during a burn-in operation as claims 9, 23, 44 disclosed, and wherein the characteristic is mobility as claims 16, 37 disclosed, and wherein the preconditioning step comprises subjecting each of cross-coupled PMOS load devices to substantially equal time durations of negative gate-to-source voltage as claims 20-22, 28-33, 41-43 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827

5/23/2006